Applicant believes the Examiner has interpreted Citron et al. in a manner inconsistent with the language and content of this reference as it would have been understood by a person of ordinary skill in the art at the filing date of the present application. In support of this position, Applicant submits herewith a declaration under 37 C.F.R. 1.132 by Daniel Citron, who is both the Applicant and the lead author of Citron et al. The declaration shows clearly that the person of ordinary skill would have understood the reference as relating exclusively to the use of Bus-Expanders on off-chip buses. Applicant believes the declaration should be entered, notwithstanding the final rejection of the claims, because it will clarify the outstanding issues in the case for purposes of allowance or appeal, without requiring that the Examiner perform any further search.

Furthermore, even if it were conceded, for the sake of argument, that Citron et al. describes the use of on-chip Bus-Expanders, this reference still neither teaches nor suggests the added element of independent claims 1 and 14: that a table in the L1 cache for use in compaction of address fields is shared by the address bus expanders that are coupled to the first and third buses. The first bus, according to the claims, connects the L1 cache to the processing component, while the third bus connects the L1 cache to the L2 cache. These are, in other words, two different buses, connecting the L1 cache to two different destinations, but they share the same table for compaction of address field.

Citron et al. neither teaches nor suggests this sort of table sharing. In relation to this element of claim 1, the Examiner referred to the address-LUT and data-LUT mentioned on page 96 of Citron et al. These elements in Citron et al., however, cannot possibly correspond to the elements of claim 1 because:

1. They both connect the same cache to the same memory, rather than connecting a cache to two different destinations as in claim 1.
2. The cited passage explicitly uses two different tables (address-LUT and data-LUT), not a shared table as in claim 1.
3. Since one of the buses is a data bus, it cannot possibly use a table for compaction of address fields, as recited in claim 1. Only the address bus can use the address-LUT.

These differences are in addition to the fact that the buses in question are off-chip, as noted above.

Thus, claims 1 and 14 are believed to be patentable over the cited art. In view of the patentability of these independent claims, dependent claims 2-12 and 15-26 are also believed to be patentable.

Applicant believes the remarks presented above to be fully responsive to all of the objections and grounds of rejection raised by the Examiner. In view of these remarks, all of the claims now pending in this application are believed to be in condition for allowance. Prompt notice to this effect is requested.

Please charge any fees associated with this paper to deposit account No. 09-0468.

Respectfully submitted,

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